

**PATENT APPLICATION  
DOCKET NO. 1726.7220800**

In the United States Patent and Trademark Office

**FILING OF A UNITED STATES PATENT APPLICATION**

**Title:**

**METHOD AND APPARATUS FOR EVALUATING AND CALIBRATING A  
SIGNALING SYSTEM**

**Inventors:**

<b>Jared Zerbe</b>	<b>Pak Chau</b>
<b>William F. Stonecypher</b>	

**Attorney of Record  
Ross D. Snyder, Reg. No. 37,730  
115 Wild Basin Road, Suite 107  
Austin, Texas 78746  
Phone (512) 347-9223  
Fax (512) 347-9224**

Express Mail Label No.

**Date of Deposit:**

I hereby certify that this paper is being deposited with the U.S. Postal Service "Express Mail Post Office to Addresses" service under 37 C.F.R. Section 1.10 on the 'Date of Deposit', indicated above, and is addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231.

**Name of Depositor:**

(print or type)

Signature: \_\_\_\_\_

## Technical Field of the Invention

The invention relates generally to communication systems and, more specifically, to *in-situ* testing of communications systems.

5

## Background of the Invention

For information communication and processing systems to operate reliably, it is important to be able to test these systems and measure various performance characteristics that pertain to them. Classically, it has been very difficult to observe the fidelity of a signaling system from a transmit circuit to a receive circuit, including a medium through which the transmit circuit is coupled to the receive circuit. It has been especially difficult to obtain *in-situ* measurements of the operation of the system. Rather, external test equipment is typically introduced into the system for the purpose of obtaining measurements. It is common for an external signal generator, for example one capable of producing test signals with ultrafast or adjustable transition times, and an external measurement device, such as an oscilloscope, to be connected to a system under test. However, since such external test equipment has characteristics different from system under test, measurements derived using the external test equipment may not accurately reflect the actual performance of the system under test.

While it was possible to obtain meaningful information from simpler systems of the past using external test equipment, the increasing complexity and operating frequencies of modern systems introduce additional complications that impair the effectiveness of testing using external test equipment. For example, much higher frequencies and controlled impedances make it much harder to introduce external test equipment without distorting the signals being measured and, therefore, affecting the measurements themselves. Moreover, connection and disconnection of the external test equipment requires time, effort, and, potentially, additional design considerations, such as the provision of test points within a system. Also, external test equipment does not allow testing to be performed from the perspective of the actual receive circuit within the

system. Thus, such testing cannot definitively provide information as to what the receive circuit actually receives. Therefore, traditional testing techniques fail to provide complete and accurate information about the system under test. Thus, a technique is needed to provide complete and accurate information about a system under test and to enable *in-situ* testing of the system.

## Brief Description of the Drawings

Figure 1 is a block diagram illustrating a signaling system in accordance with an embodiment of the invention.

5

Figure 2 is a logic diagram illustrating a prior art transmit circuit.

Figure 3 is a logic diagram illustrating a prior art receive circuit.

10

Figure 4 is a logic diagram illustrating a transmit circuit capable of operating in a PRBS test mode in accordance with an embodiment of the invention.

Figure 5 is a logic diagram illustrating a receive circuit capable of operating in a PRBS test mode in accordance with an embodiment of the invention.

15

Figure 6 is a logic diagram illustrating a transmit circuit capable of operating in a PRBS test mode and a roll test mode in accordance with an embodiment of the invention.

Figure 7 is a logic diagram illustrating a receive circuit capable of operating in a PRBS test mode and a roll test mode in accordance with an embodiment of the invention.

20

Figure 8 is a logic diagram illustrating a prior art quad Rambus signaling level (QRSL) transmit circuit.

25

Figure 9 is a logic diagram illustrating a quad Rambus signaling level (QRSL) transmit circuit capable of operating in a PRBS test mode in accordance with an embodiment of the invention.

30

Figure 10 is a logic diagram illustrating a quad Rambus signaling level (QRSL) transmit circuit capable of operating in a PRBS mode and a roll test mode in accordance with an embodiment of the present invention.

Figure 11 is a logic diagram illustrating a prior art quad Rambus signaling level (QRSL) receive circuit. Pad 1101 is coupled to node 1102, which is coupled to even receiver 1105 and to odd receiver 1106.

5

Figure 12 is a logic diagram illustrating a quad Rambus signaling level (QRSL) receive circuit capable of operating in a PRBS test mode in accordance with an embodiment of the invention.

10        Figure 13 is a logic diagram illustrating a quad Rambus signaling level (QRSL) receive circuit capable of operating in a PRBS test mode and a roll test mode in accordance with an embodiment of the invention.

15        Figure 14 is a timing diagram illustrating signals in accordance with an embodiment of the invention.

Figure 15 is a block diagram illustrating a differential receiver that may be used in conjunction with an embodiment of the invention.

20        Figure 16 is a waveform diagram illustrating a differential signal that may be used in conjunction with an embodiment of the invention.

Figure 17 is a waveform diagram illustrating a differential signal that may be used in conjunction with an embodiment of the invention.

25

Figure 18 is a waveform diagram illustrating a differential signal that may be used in conjunction with an embodiment of the invention.

30        Figure 19 is a schematic diagram illustrating an example of an input stage of an offsetable differential receiver in accordance with an embodiment of the invention.

Figure 20 is a schematic diagram illustrating an example of an input stage of an offsetable differential receiver in accordance with an embodiment of the invention.

Figure 21 is a waveform diagram illustrating the shifting of an offset for a differential signal in accordance with an embodiment of the invention.

Figure 22 is a waveform diagram illustrating a waveform obtained by determining a difference between waveforms.

Figure 23 is a flow diagram illustrating a method in accordance with an embodiment of the invention.

Figure 24 is a waveform diagram illustrating an example of a persistent display of overlapping samples of a waveform in accordance with an embodiment of the invention.

Figure 25 is a waveform diagram illustrating an example of a persistent display of overlapping samples of a waveform in accordance with an embodiment of the invention.

Figure 26 is a waveform diagram illustrating an example of a persistent display of overlapping samples of a waveform in accordance with an embodiment of the invention.

Figure 27 is a waveform diagram illustrating an example of a persistent display of overlapping samples of a waveform in accordance with an embodiment of the invention.

Figure 28 is a waveform diagram illustrating an example of a persistent display of overlapping samples of a waveform in accordance with an embodiment of the invention.

Figure 29 is a waveform diagram illustrating an example of a persistent display of overlapping samples of a waveform in accordance with an embodiment of the invention.

Figure 30 is a block diagram illustrating a system in accordance with an embodiment of the invention.

Figure 31 is a flow diagram illustrating a method in accordance with an  
5 embodiment of the invention.

## Detailed Description of a Preferred Embodiment

A method and apparatus for evaluating and calibrating a signaling system is described. Evaluation is accomplished using the same circuits actually involved in normal operation of the signaling system. Such circuits are adapted to provide testing capability with minimal additional complexity. Thus, capability for *in-situ* testing of a signaling system is provided, and information may be obtained from the actual perspective of a receive circuit in the system. Both the need for the introduction of external test equipment and the inaccuracy caused by its introduction are avoided. An embodiment of the invention may be implemented to provide a built-in self-test (BIST) capability within an operational system. Such capability can be very beneficial, especially where access to internal components of a system would otherwise be difficult. For example, in addition to being applicable to signaling systems where the transmit circuit is located separately from the receive circuit, an embodiment of the invention may be applied to a relatively closed system, for example, a system fabricated as an integrated circuit. Thus, even when an integrated circuit is packaged, extensive internal evaluation and optimization capability may be provided in accordance with the invention.

A pattern of test information is generated in a transmit circuit of the system and is transmitted to a receive circuit. A similar pattern of information is generated in the receive circuit and used as a reference. The receive circuit receives the pattern of test information generated in the transmit circuit and compares it to the pattern of information generated in the receive circuit. Any differences between the patterns are observable. Preferably, the patterns are repeating patterns that allow many iterations of testing to be performed. Thus, even events that occur infrequently within the system may be observed.

In one embodiment, a linear feedback shift register (LFSR) is implemented to produce patterns. Information obtained from testing may be used to assess the effects of various system parameters, including but not limited to output current, crosstalk cancellation coefficients, and self-equalization coefficients, and system parameters may



be adjusted to optimize system performance. Embodiments of the invention may be used in assessing a wide variety of phenomena, including, but not limited to, overshoot, undershoot, edge rates, crosstalk, duty cycle error (including the cumulative duty cycle error across the transmit circuit, the medium, and the receive circuit), impedance continuity/discontinuity, and the effectiveness of different receive and transmit effects. An embodiment of the invention may be practiced with various types of signaling systems, including those with single-ended signals and those with differential signals. An embodiment of the invention may be applied to systems communicating a single bit of information on a single conductor at a given time and to systems communicating multiple bits of information on a single conductor simultaneously.

Figure 1 is a block diagram illustrating a signaling system in accordance with an embodiment of the invention. The system comprises transmit circuit 101, medium 102, and receive circuit 103. Transmit circuit 101 comprises shift register 105 and test loop 106. Transmit circuit 101 can operate in a normal mode or a test mode. In the normal mode, shift register 105 receives a data via a data input 104, which may be a parallel or serial data input. Shift register 105 shifts the bits of the data to the right, providing each bit as a output at the interface with medium 102.

The data are transmitted across medium 102 to receive circuit 103. In addition to providing output to medium 102, shift register 105 also provides its output to test loop 106. Test loop 106 provides an input 107 to shift register 105. In the test mode, shift register 105 and test loop 106 function to generate a test pattern for transmission over medium 102. The test pattern is preferably, although not necessarily a repeating pattern. Test loop 106 may be a simple loop, such as a loop of wire, or it may include other combinational and/or sequential logic. For example, it may include logic gates such as AND, OR, NAND, NOR, XOR, and/or XNOR gates. Such gates may be used to implement an LFSR. An LFSR is capable of producing maximal-length repeating patterns with a minimum of additional complexity. The LFSR can produce pseudo-random bit sequences (PRBS), which may be beneficially applied to testing the system under a wide variety of logical conditions.

Receive circuit 103 includes shift register 108 and test loop 111. In the normal mode, receive circuit 103 receives data from the transmit circuit 101 via medium 102, which may, as one example, be an electrical conductor coupling the transmit circuit 101 to the receive circuit 103. The bits of the data are shifted through shift register 108 and provided at data output 109.

As appropriate, the transmit circuit 101 may include a transmitter 115 coupled to medium 102 and the receive circuit 103 may include a receiver 116 coupled to the medium 102. In that case, an output of shift register 105 is coupled to an input of transmitter 115 and to an input of test loop 106. The output of transmitter 115 is coupled to medium 102. Medium 102 is coupled to an input of receiver 116. A receive clock signal is provided at input 117 of receiver 116. A voltage reference signal is provided at input 118 of receiver 116. Both the receive clock signal at input 117 and the voltage reference signal may be varied over a wide range to allow testing of the system under a wide variety of conditions.

Transmitter 115 may be any suitable transmitter. An example includes, but is not limited to, a driver circuit for driving signals onto medium 102. The driver circuit may provide desirable characteristics, for example, a controlled source impedance and well-defined transition times. Transmitter 115 may provide a single-ended signal or a differential signal over medium 102. Transmitter 115 may be able to communicate one or more bits of information over a single conductor simultaneously.

Likewise, receiver 116 may be any suitable receiver. An example includes, but is not limited to, a receiver for determining digital signaling levels of signals present on medium 102. Receiver 116 may provide desirable characteristics, for example, one or more voltage or current level thresholds, controlled hysteresis, and controlled timing. Receiver 116 may be configured to receive a single-ended signal or a differential signal from medium 102. Receiver 116 may be able to receive one or more bits of information over a single conductor simultaneously.

While subsequent Figures, for example, Figures 4, 6, 9, and 10 are illustrated without a transmitter such as transmitter 115, the embodiments of these Figures may be implemented with such a transmitter. While subsequent Figures, for example, Figures 5, 7, 12, and 13 are illustrated with a receiver such as receiver 116, the embodiments of these Figures may be implemented with such a receiver.

Shift register 108 is coupled to test loop 111 via coupling 110. The output of the test loop 111 is coupled back to an input of shift register 108 and also to an input of comparison circuit 113, which may, as one example, be implemented using an XOR logic gate. Another input of the comparison circuit 113 is coupled to medium 102 and receives the test pattern transmitted by transmit circuit 101 over medium 102. Comparison circuit 113 provides a comparison output 114. In the test mode, shift register 108 and test loop 111 operate to produce a pattern identical to or deterministically related to the pattern produced by transmit circuit 101. Comparison circuit 113 compares the pattern generated in the transmit circuit 101 to the pattern generated in the receive circuit 103 to determine for each bit whether the patterns match. To establish a relationship between the pattern produced by the transmit circuit 101 and the pattern produced by the receive circuit 103, information to synchronize the pattern of the receive circuit 103 with the pattern of the transmit circuit 101 may be communicated from the transmit circuit 101 to the receive circuit 103, and elements of the receive circuit may be preloaded with such information.

The system may be operated in roll test mode. In the roll test mode, the patterns need not necessarily match, as long as they are repeatable. In the roll test mode, the system operates as a "repeatability detector." The roll test mode generates repeating patterns, and, upon comparison, any variation from the repeating patterns is detected. Thus, the pattern generated by the transmit circuit and the pattern generated by the receive circuit need not be the same. In fact, the receive circuit need not be preloaded with information to synchronize its pattern with that of the transmit circuit.

In the roll test mode, the timing of receiver 116 may be adjusted, for example, swept over a range, by varying the receive clock signal at node 117, and the symbol thresholds of receiver 116 may be adjusted, for example, swept over a range, by varying the voltage reference signal at node 118. While the voltage reference signal is stated in terms of voltage, it may be implemented to allow adjustment of other electrical parameters relating to reception of signals at receiver 116.

Figure 2 is a logic diagram illustrating a prior art transmit circuit. Node 201 is coupled to a serial data input of a shift register comprising flip-flops 215, 217, 219, and 221. A load signal for performing a parallel data load of the shift register is provided to the shift register at node 203. A transmit clock signal is provided to a clock input of the shift register at node 205. Nodes 207, 209, 211, and 213 are coupled to parallel load data inputs of flip-flops 215, 217, 219, and 221, respectively. The serial data output of the shift register at the output of flip-flop 221 is coupled to node 223, which is coupled to an input of multiplexer 226.

Node 202 is coupled to a serial data input of a shift register comprising flip-flops 216, 218, 220, and 222. A load signal for performing a parallel data load of the shift register is provided to the shift register at node 204. A transmit clock signal is provided to a clock input of the shift register at node 206. Nodes 208, 210, 212, and 214 are coupled to parallel load data inputs of flip-flops 216, 218, 220, and 222, respectively. The serial data output of the shift register at the output of flip-flop 222 is coupled to node 224, which is coupled to an input of multiplexer 226.

A transmit clock signal is provided to an input of multiplexer 226 at node 225. The output of multiplexer 226 is coupled to node 230, which is coupled to an input of output driver 227. An output of output driver 227 is coupled to node 228, which is coupled to pad 229.

Figure 3 is a logic diagram illustrating a prior art receive circuit. Pad 301 is coupled to node 302, which is coupled to an input of even receiver 305 and to an input of

odd receiver 306. A receive clock signal is provided to an input of even receiver 305 at node 303 and to an input of odd receiver 306 at node 304. An output of even receiver 305 at node 307 is coupled to an input of a shift register comprising flip-flops 313, 315, 317, and 319. A receive clock is provided to a clock input of the shift register at node 309. An unload signal for providing parallel data outputs from the shift register is applied to the shift register via node 311. Parallel data are provided at parallel data outputs 321, 323, 325, and 327 of flip-flops 313, 315, 317, and 319, respectively.

An output of even receiver 306 at node 308 is coupled to an input of a shift register comprising flip-flops 314, 316, 318, and 320. A receive clock is provided to a clock input of the shift register at node 310. An unload signal for providing parallel data outputs from the shift register is applied to the shift register via node 312. Parallel data are provided at parallel data outputs 322, 324, 326, and 328 of flip-flops 314, 316, 318, and 320, respectively.

Figure 4 is a logic diagram illustrating a transmit circuit capable of operating in a PRBS test mode in accordance with an embodiment of the invention. Node 401 is coupled to a serial data input of a shift register comprising flip-flops 415, 417, 419, and 421. A load signal for performing a parallel data load of the shift register is provided to the shift register at node 403. A transmit clock signal is provided to a clock input of the shift register at node 405. Nodes 407, 409, 411, and 413 are coupled to parallel load data inputs of flip-flops 415, 417, 419, and 421, respectively.

The serial data output of the shift register at the output of flip-flop 421 is coupled to node 423, which is coupled to an input of multiplexer 426. Node 423 is also coupled to an input of XOR gate 433. A signal at node 431 taken from the data output of flip-flop 417 is coupled to an input of XOR gate 433. The output of XOR gate 433 is coupled to an input of multiplexer 446 via node 435. A fixed logic zero signal is coupled to an input of multiplexer 446 at node 442. A PRBS test signal is coupled to a selection input of multiplexer 446 via node 444. The output of multiplexer 446 is coupled to node 402.

Node 402 is coupled to a serial data input of a shift register comprising flip-flops 416, 418, 420, and 422. A load signal for performing a parallel data load of the shift register is provided to the shift register at node 404. A transmit clock signal is provided to a clock input of the shift register at node 406. Nodes 408, 410, 412, and 414 are  
5 coupled to parallel load data inputs of shift registers 416, 418, 420, and 422, respectively.

Node 424 is taken from a serial data output of the shift register at the output of flip-flop 422 and is coupled to an input of multiplexer 426 and to an input of XOR gate 434. A signal at node 432 taken from the data output of flip-flop 418 is coupled to an  
10 input of XOR gate 434. The output of XOR gate 434 appears at node 436, which is coupled to an input of flip-flop 438.

A transmit clock signal is provided to a clock input of flip-flop 438 via node 437. An output of flip-flop 438 is coupled to an input of multiplexer 445 via node 439. A  
15 fixed logic zero input is coupled to an input of multiplexer 445 at node 441. A PRBS test signal is coupled to a selection input of multiplexer 445 via node 443. An output of multiplexer 445 is coupled to node 401.

A transmit clock signal is provided to multiplexer 426 via node 425. The output  
20 of multiplexer of 426 is coupled via node 430 to an input of output driver 427. Output driver 427 provides an output at node 428, which is coupled to pad 429.

Figure 5 is a logic diagram illustrating a receive circuit capable of operating in a PRBS test mode in accordance with an embodiment of the invention. Pad 501 is coupled  
25 to node 502, which is coupled to even receiver 505 and odd receiver 506. A receive clock signal is provided to even receiver 505 at node 503 and to odd receiver 506 at node 504.

An output of even receiver 505 is coupled to an input of multiplexer 543 and to an  
30 input of XOR gate 547 via node 507. The output of multiplexer 543 is coupled to an input of XOR gate 547 and to a serial data input of a shift register comprising flip-flops

513, 515, 517, and 519 via node 545. An output of XOR gate 547 is coupled to an input of OR gate 551 at node 549.

5 A receive clock signal is provided to a clock input of the shift register via node 509. An unload signal for providing parallel data outputs from the shift register is applied to the shift register via node 511. Parallel data are provided at parallel data outputs 521, 523, 525, and 527 of flip-flops 513, 515, 517, and 519, respectively.

10 An output of flip-flop 519 is coupled to an input of XOR gate 533 via node 529. An output of flip-flop 515 is coupled to an input of XOR gate 533 via node 531. An output of XOR gate 533 is coupled to an input of multiplexer 544 via node 535. A PRBS test signal is applied to a selection input 542 of multiplexer 544.

15 An output of odd receiver 506 is coupled to an input of multiplexer 544 and to an input of XOR gate 548 via node 508. The output of multiplexer 544 is coupled to an input of XOR gate 548 and to the serial data input of a shift register comprising flip-flops 514, 516, 518, and 520 via node 546. An output of XOR gate 548 is coupled to an input of OR gate 551 at node 550.

20 A receive clock signal is provided to a clock input of the shift register via node 510. An unload signal for providing parallel data outputs from the shift register is applied to the shift register via node 512. Parallel data are provided at parallel data outputs 522, 524, 526, and 528 of flip-flops 514, 516, 518, and 520, respectively.

25 An output of flip-flop 520 is coupled to an input of XOR gate 534 via node 530. An output of flip-flop 516 is coupled to an input of XOR gate 534 via node 532. An output of XOR gate 534 is coupled to an input of flip-flop 538 via node 536. A receive clock signal is applied to a clock input 537 of flip-flop 538. An output of flip-flop 538 is coupled to an input of multiplexer 543 via node 539. A PRBS test signal is applied to a  
30 selection input 541 of multiplexer 543.

An output of OR gate 551 at node 552 is coupled to an input of flip-flop 555. A receive clock signal is provided to a clock input of flip-flop 555 at node 553. A PRBS test signal is applied to an input of flip-flop 555 at node 554. An error flag output of flip-flop 555 is provided at node 556.

5

Figure 6 is a logic diagram illustrating a transmit circuit capable of operating in a PRBS test mode and a roll test mode in accordance with an embodiment of the invention. Node 601 is coupled to a serial data input of a shift register comprising flip-flops 615, 617, 619, and 621. A load signal for performing a parallel data load of the shift register is provided to the shift register at node 603. A transmit clock signal is provided to a clock input of the shift register at node 605. Nodes 607, 609, 611, and 613 are coupled to parallel load data inputs of flip-flops 615, 617, 619, and 621, respectively.

The serial data output of the shift register at the output of flip-flop 621 is coupled to node 623, which is coupled to an input of multiplexer 626. Node 623 is also coupled to an input of XOR gate 633 and to an input of multiplexer 645. A signal at node 631 taken from the data output of flip-flop 617 is coupled to an input of XOR gate 633. The output of XOR gate 633 is coupled to an input of multiplexer 646 via node 635. A fixed logic zero signal is coupled to an input of multiplexer 646 at node 642. A PRBS test signal is coupled to a selection input of multiplexer 646 via node 644. A roll test signal is coupled to an input of multiplexer 646 via node 648. The output of multiplexer 646 is coupled to node 602.

Node 602 is coupled to a serial data input of a shift register comprising flip-flops 616, 618, 620, and 622. A load signal for performing a parallel data load of the shift register is provided to the shift register at node 604. A transmit clock signal is provided to a clock input of the shift register at node 606. Nodes 608, 610, 612, and 614 are coupled to parallel load data inputs of shift registers 616, 618, 620, and 622, respectively.

Node 624 is taken from a serial data output of the shift register at the output of flip-flop 622 and is coupled to an input of multiplexer 626, an input of XOR gate 634,



and an input of multiplexer 646. A signal at node 632 taken from the data output of flip-flop 618 is coupled to an input of XOR gate 634. The output of XOR gate 634 appears at node 636, which is coupled to an input of flip-flop 638.

5           A transmit clock signal is provided to a clock input of flip-flop 638 via node 637. An output of flip-flop 638 is coupled to an input of multiplexer 645 via node 639. A fixed logic zero input is coupled to an input of multiplexer 645 at node 641. A PRBS test signal is coupled to a selection input of multiplexer 645 via node 643. A roll test signal is coupled to a selection input of multiplexer 645 via node 647. An output of multiplexer  
10   645 is coupled to node 601.

          A transmit clock signal is provided to multiplexer 626 via node 625. The output of multiplexer of 626 is coupled via node 630 to an input of output driver 627. Output driver 627 provides an output at node 628, which is coupled to pad 629.

15           Figure 7 is a logic diagram illustrating a receive circuit capable of operating in a PRBS test mode and a roll test mode in accordance with an embodiment of the invention. Pad 701 is coupled to node 702, which is coupled to even receiver 705 and odd receiver 706. A receive clock signal is provided to even receiver 705 at node 703 and to odd  
20   receiver 706 at node 704.

          An output of even receiver 705 is coupled to an input of multiplexer 743 and to an input of XOR gate 747 via node 707. The output of multiplexer 743 is coupled to an input of XOR gate 747 and to a serial data input of a shift register comprising flip-flops  
25   713, 715, 717, and 719 via node 745. An output of XOR gate 747 is coupled to an input of OR gate 751 at node 749.

          A receive clock signal is provided to a clock input of the shift register via node 709. An unload signal for providing parallel data outputs from the shift register is  
30   applied to the shift register via node 711. Parallel data are provided at parallel data outputs 721, 723, 725, and 727 of flip-flops 713, 715, 717, and 719, respectively.

An output of flip-flop 719 is coupled to an input of XOR gate 733 and to an input of multiplexer 743 via node 729. An output of flip-flop 715 is coupled to an input of XOR gate 733 via node 731. An output of XOR gate 733 is coupled to an input of multiplexer 744 via node 735. A PRBS test signal is applied to a selection input 742 of multiplexer 744. A roll test signal is applied to a selection input 788 of multiplexer 744.

An output of odd receiver 706 is coupled to an input of multiplexer 744 and to an input of XOR gate 748 via node 708. The output of multiplexer 744 is coupled to an input of XOR gate 748 and to the serial data input of a shift register comprising flip-flops 714, 716, 718, and 720 via node 746. An output of XOR gate 748 is coupled to an input of OR gate 751 at node 750.

A receive clock signal is provided to a clock input of the shift register via node 710. An unload signal for providing parallel data outputs from the shift register is applied to the shift register via node 712. Parallel data are provided at parallel data outputs 722, 724, 726, and 728 of flip-flops 714, 716, 718, and 720, respectively.

An output of flip-flop 720 is coupled to an input of XOR gate 734 and to an input of multiplexer 744 via node 730. An output of flip-flop 716 is coupled to an input of XOR gate 734 via node 732. An output of XOR gate 734 is coupled to an input of flip-flop 738 via node 736. A receive clock signal is applied to a clock input 737 of flip-flop 738. An output of flip-flop 738 is coupled to an input of multiplexer 743 via node 739. A PRBS test signal is applied to a selection input 741 of multiplexer 743. A roll test signal is applied to a selection input 787 of multiplexer 743.

An output of OR gate 751 at node 752 is coupled to an input of flip-flop 755. A receive clock signal is provided to a clock input of flip-flop 755 at node 753. A PRBS test or roll test signal is applied to an input of flip-flop 755 at node 754. An error flag output of flip-flop 755 is provided at node 756.

While the circuit may be implemented to receive single-ended signals at pad 701, the circuit may also be implemented to receive differential signals. Pad 757, which is coupled to node 758, which, in turn, is coupled to an input of even receiver 705 and to an input of odd receiver 706 may be used together with pad 701 to receive the differential signals.

Figure 8 is a logic diagram illustrating a prior art quad Rambus signaling level (QRSL) transmit circuit. A fixed logic zero signal is coupled at node 801 to an input of a shift register comprising flip-flops 815, 817, 819, and 821. A load signal for performing a parallel data load of the shift register is provided to the shift register at node 803. A transmit clock signal is provided to a clock input of the shift register at node 805. Nodes 807, 809, 811, and 813 are coupled to parallel load data inputs of flip-flops 815, 817, 819, and 821, respectively. A serial data output the shift register at the output of flip-flop 821 is coupled to an input of multiplexer 826 at node 823.

A fixed logic zero signal is coupled at node 802 to an input of a shift register comprising flip-flops 816, 818, 820, and 822. A load signal for performing a parallel data load of the shift register is provided to the shift register at node 804. A transmit clock signal is provided to a clock input of the shift register at node 806. Nodes 808, 810, 812, and 814 are coupled to parallel load data inputs of flip-flops 816, 818, 820, and 822, respectively. A serial data output the shift register at the output of flip-flop 822 is coupled to an input of multiplexer 826 at node 824.

A fixed logic zero signal is coupled at node 851 to an input of a shift register comprising flip-flops 865, 867, 869, and 871. A load signal for performing a parallel data load of the shift register is provided to the shift register at node 853. A transmit clock signal is provided to a clock input of the shift register at node 855. Nodes 857, 859, 861, and 863 are coupled to parallel load data inputs of flip-flops 865, 867, 869, and 871, respectively. A serial data output the shift register at the output of flip-flop 871 is coupled to an input of multiplexer 876 at node 873.

A fixed logic zero signal is coupled at node 852 to an input of a shift register comprising flip-flops 866, 868, 870, and 872. A load signal for performing a parallel data load of the shift register is provided to the shift register at node 854. A transmit clock signal is provided to a clock input of the shift register at node 856. Nodes 858, 860, 862, and 864 are coupled to parallel load data inputs of flip-flops 866, 868, 870, and 872, respectively. A serial data output the shift register at the output of flip-flop 872 is coupled to an input of multiplexer 876 at node 874.

A transmit clock signal is provided to multiplexer 826 via node 825. The output of multiplexer of 826 is coupled via node 830 to an input of output driver 827. A transmit clock signal is coupled to an input of multiplexer of 876 via node 875. The output of multiplexer 876 is coupled to output driver 827 via node 880. Output driver 827 provides an output at node 828, which is coupled to pad 829.

Figure 9 is a logic diagram illustrating a quad Rambus signaling level (QRSL) transmit circuit capable of operating in a PRBS test mode in accordance with an embodiment of the invention. Node 901 is coupled to a serial data input of a shift register comprising flip-flops 915, 917, 919, and 921. A load signal for performing a parallel data load of the shift register is provided to the shift register at node 903. A transmit clock signal is provided to a clock input of the shift register at node 905. Nodes 907, 909, 911, and 913 are coupled to parallel load data inputs of flip-flops 915, 917, 919, and 921, respectively.

The serial data output of the shift register at the output of flip-flop 921 is coupled to node 923, which is coupled to an input of multiplexer 926. Node 923 is also coupled to an input of XOR gate 933. A signal at node 931 taken from the data output of flip-flop 915 is coupled to an input of XOR gate 933. The output of XOR gate 933 is coupled to an input of multiplexer 946 via node 935. A fixed logic zero signal is coupled to an input of multiplexer 946 at node 942. A PRBS test signal is coupled to a selection input of multiplexer 946 via node 944. The output of multiplexer 946 is coupled to node 902.

Node 902 is coupled to a serial data input of a shift register comprising flip-flops 916, 918, 920, and 922. A load signal for performing a parallel data load of the shift register is provided to the shift register at node 904. A transmit clock signal is provided to a clock input of the shift register at node 906. Nodes 908, 910, 912, and 914 are  
5 coupled to parallel load data inputs of shift registers 916, 918, 920, and 922, respectively.

Node 924 is taken from a serial data output of the shift register at the output of flip-flop 922 and is coupled to an input of multiplexer 926 and to an input of XOR gate 934. A signal at node 932 taken from the data output of flip-flop 916 is coupled to an  
10 input of XOR gate 934. The output of XOR gate 934 appears at node 936, which is coupled to an input of multiplexer 995. A fixed logic zero signal is coupled to an input of multiplexer 995 via node 991. A PRBS test signal is coupled to a selection input of multiplexer 995 via node 993. An output of multiplexer 995 is coupled to node 951.

Node 951 is coupled to a serial data input of a shift register comprising flip-flops 965, 967, 969, and 971. A load signal for performing a parallel data load of the shift register is provided to the shift register at node 953. A transmit clock signal is provided to a clock input of the shift register at node 955. Nodes 957, 959, 961, and 963 are  
15 coupled to parallel load data inputs of flip-flops 965, 967, 969, and 971, respectively.

Node 973 is taken from the serial data output of the shift register at the output of flip-flop 971 and is coupled to an input of multiplexer 976 and to an input of XOR gate 983. Node 981 provides a signal taken from the data output of flip-flop of 965 and provides it to an input of XOR gate 983. The output of XOR gate 983 appears at node  
20 985 and is coupled to an input of multiplexer of 996. A fixed logic zero signal is coupled to an input of multiplexer 996 via input 992. A PRBS test signal is coupled to a selection input of multiplexer 996 via node 994. The output of multiplexer 996 is coupled to node 952.

Node 952 is coupled to a serial data input of a shift register comprising flip-flops 966, 968, 970, and 972. A load signal for performing a parallel data load of the shift  
30

register is provided to the shift register at node 954. A transmit clock signal is provided to a clock input of the shift register at node 956. Nodes 958, 960, 962, and 964 are coupled to parallel load data inputs of flip-flops 966, 968, 970, and 972, respectively.

5        Node 974 provides a signal taken from the serial data output of the shift register at the output of flip-flop 972 to an input of multiplexer 976 and to an input of XOR gate 984. Node 982 is taken from a data output of flip-flop 966 and coupled to an input of XOR gate 984. XOR gate 984 provides an output at node 986, which is coupled to an input of flip-flop 938.

10        A transmit clock signal is provided to a clock input of flip-flop 938 via node 937. A PRBS test input signal is provided to an inverted input of flip-flop 938 via node 949. An output of flip-flop 938 is coupled to an input of multiplexer 945 via node 939. A fixed logic zero input is coupled to an input of multiplexer 945 at node 941. A PRBS test  
15        signal is coupled to a selection input of multiplexer 945 via node 943. An output of multiplexer 945 is coupled to node 901.

20        A transmit clock signal is provided to multiplexer 926 via node 925. The output of multiplexer 926 is coupled via node 930 to an input of output driver 927. A transmit clock signal is coupled to an input of multiplexer 976 via node 975. The output of multiplexer 976 is coupled to output driver 927 via node 980. Output driver 927 provides an output at node 928, which is coupled to pad 929.

25        Figure 10 is a logic diagram illustrating a quad Rambus signaling level (QRSL) transmit circuit capable of operating in a PRBS mode and a roll test mode in accordance with an embodiment of the present invention. Node 1001 is coupled to a serial data input of a shift register comprising flip-flops 1015, 1017, 1019, and 1021. A load signal for performing a parallel data load of the shift register is provided to the shift register at node 1003. A transmit clock signal is provided to a clock input of the shift register at node  
30        1005. Nodes 1007, 1009, 1011, and 1013 are coupled to parallel load data inputs of flip-flops 1015, 1017, 1019, and 1021, respectively.

The serial data output of the shift register at the output of flip-flop 1021 is coupled to node 1023, which is coupled to an input of multiplexer 1026. Node 1023 is also coupled to an input of XOR gate 1033 and to an input of multiplexer 1045. A signal at node 1031 taken from the data output of flip-flop 1015 is coupled to an input of XOR gate 1033. The output of XOR gate 1033 is coupled to an input of multiplexer 1046 via node 1035. A fixed logic zero signal is coupled to an input of multiplexer 1046 at node 1042. A PRBS test signal is coupled to a selection input of multiplexer 1046 via node 1044. A roll test signal is coupled to an input of multiplexer 1046 via node 1048. The output of multiplexer 1046 is coupled to node 1002.

Node 1002 is coupled to a serial data input of a shift register comprising flip-flops 1016, 1018, 1020, and 1022. A load signal for performing a parallel data load of the shift register is provided to the shift register at node 1004. A transmit clock signal is provided to a clock input of the shift register at node 1006. Nodes 1008, 1010, 1012, and 1014 are coupled to parallel load data inputs of shift registers 1016, 1018, 1020, and 1022, respectively.

Node 1024 is taken from a serial data output of the shift register at the output of flip-flop 1022 and is coupled to an input of multiplexer 1026, an input of XOR gate 1034, and an input of multiplexer 1046. A signal at node 1032 taken from the data output of flip-flop 1016 is coupled to an input of XOR gate 1034. The output of XOR gate 1034 appears at node 1036, which is coupled to an input of multiplexer 1095. A fixed logic zero signal is coupled to an input of multiplexer 1095 via node 1091. A PRBS test signal is coupled to a selection input of multiplexer 1095 via node 1093. A roll test signal is coupled to a selection input of multiplexer of 1095 via node 1097. An output of multiplexer 1095 is coupled to node 1051.

Node 1051 is coupled to a serial data input of a shift register comprising flip-flops 1065, 1067, 1069, and 1071. A load signal for performing a parallel data load of the shift register is provided to the shift register at node 1053. A transmit clock signal is provided

to a clock input of the shift register at node 1055. Nodes 1057, 1059, 1061, and 1063 are coupled to parallel load data inputs of flip-flops 1065, 1067, 1069, and 1071, respectively.

5           Node 1073 is taken from the serial data output of the shift register at the output of flip-flop 1071 and is coupled to an input of multiplexer 1076, to an input of XOR gate 1083, and to an input of multiplexer 1095. Node 1081 provides a signal taken from the data output of flip-flop of 1065 and provides it to an input of XOR gate 1083. The output of XOR gate 1083 appears at node 1085 and is coupled to an input of multiplexer of  
10   1096. A fixed logic zero signal is coupled to an input of multiplexer 1096 via input 1092. A PRBS test signal is coupled to a selection input of multiplexer 1096 via node 1094. A roll test signal is coupled to a selection input of multiplexer 1096 via node 1098. The output of multiplexer 1096 is coupled to node 1052.

15           Node 1052 is coupled to a serial data input of a shift register comprising flip-flops 1066, 1068, 1070, and 1072. A load signal for performing a parallel data load of the shift register is provided to the shift register at node 1054. A transmit clock signal is provided to a clock input of the shift register at node 1056. Nodes 1058, 1060, 1062, and 1064 are coupled to parallel load data inputs of flip-flops 1066, 1068, 1070, and 1072,  
20   respectively.

Node 1074 provides a signal taken from the serial data output of the shift register at the output of flip-flop 1072 to an input of multiplexer 1076, to an input of XOR gate 1084, and to an input of multiplexer 1096. Node 1082 is taken from a data output of flip-  
25   flop 1066 and coupled to an input of XOR gate 1084. XOR gate 1084 provides an output at node 1086, which is coupled to an input of flip-flop 1038.

A transmit clock signal is provided to a clock input of flip-flop 1038 via node 1037. A PRBS test input signal is provided to an input of flip-flop 1038 via node 1049.  
30   An output of flip-flop 1038 is coupled to an input of multiplexer 1045 via node 1039. A fixed logic zero input is coupled to an input of multiplexer 1045 at node 1041. A PRBS



test signal is coupled to a selection input of multiplexer 1045 via node 1043. A roll test signal is coupled to a selection input of multiplexer 1045 via node 1047. An output of multiplexer 1045 is coupled to node 1001.

5           A transmit clock signal is provided to multiplexer 1026 via node 1025. The output of multiplexer of 1026 is coupled via node 1030 to an input of output driver 1027. A transmit clock signal is coupled to an input of multiplexer of 1076 via node 1075. The output of multiplexer 1076 is coupled to output driver 1027 via node 1080. Output driver 1027 provides an output at node 1028, which is coupled to pad 1029.

10

Figure 11 is a logic diagram illustrating a prior art quad Rambus signaling level (QRSL) receive circuit. Pad 1101 is coupled to node 1102, which is coupled to even receiver 1105 and to odd receiver 1106. A receive clock signal is provided to even receiver 1105 at node 1103 and to odd receiver 1106 at node 1104.

15

The most significant bits (MSB) from even receiver 1105 are passed to an input of a shift register comprising flip-flops 1163, 1165, 1167, and 1169 via node 1157. A receive clock signal is provided to a clock input of the shift register via node 1159. An unload signal for providing parallel data outputs from the shift register is applied to the shift register via node 1161. Parallel data are provided at parallel data outputs 1171, 1173, 1175, and 1177 of flip-flops 1163, 1165, 1167, and 1169, respectively.

20

The least significant bits (LSB) from even receiver 1105 are passed to an input of a shift register comprising flip-flops 1113, 1115, 1117, and 1119 via node 1107. A receive clock signal is provided to a clock input of the shift register via node 1109. An unload signal for providing parallel data outputs from the shift register is applied to the shift register via node 1111. Parallel data are provided at parallel data outputs 1121, 1123, 1125, and 1127 of flip-flops 1113, 1115, 1117, and 1119, respectively.

25

30           The most significant bits (MSB) from odd receiver 1106 are passed to an input of a shift register comprising flip-flops 1164, 1166, 1168, and 1170 via node 1158. A

receive clock signal is provided to a clock input of the shift register via node 1160. An unload signal for providing parallel data outputs from the shift register is applied to the shift register via node 1162. Parallel data are provided at parallel data outputs 1172, 1174, 1176, and 1178 of flip-flops 1164, 1166, 1168, and 1170, respectively.

5

The least significant bits (LSB) from even receiver 1106 are passed to an input of a shift register comprising flip-flops 1114, 1116, 1118, and 1120 via node 1108. A receive clock signal is provided to a clock input of the shift register via node 1110. An unload signal for providing parallel data outputs from the shift register is applied to the shift register via node 1112. Parallel data are provided at parallel data outputs 1122, 1124, 1126, and 1128 of flip-flops 1114, 1116, 1118, and 1120, respectively.

Figure 12 is a logic diagram illustrating a quad Rambus signaling level (QRS) receive circuit capable of operating in a PRBS test mode in accordance with an embodiment of the invention. Pad 1201 is coupled to node 1202, which is coupled to most significant bits (MSB) receiver 1205 and least significant bits (LSB) receiver 1206. A receive clock signal is provided to MSB receiver 1205 at node 1203 and to LSB receiver 1206 at node 1204.

Even-numbered bits from MSB receiver 1205 are passed to an input of multiplexer 1293 and to an input of XOR gate 1297 via node 1257. The output of multiplexer 1293 is coupled to an input of XOR gate 1297 and to a serial data input of a shift register comprising flip-flops 1263, 1265, 1267, and 1269 via node 1295. An output of XOR gate 1297 is provided at node 1299. A receive clock signal is provided to a clock input of the shift register via node 1259. An unload signal for providing parallel data outputs from the shift register is applied to the shift register via node 1261. Parallel data are provided at parallel data outputs 1271, 1273, 1275, and 1277 of flip-flops 1263, 1265, 1267, and 1269, respectively.

An output of flip-flop 1269 is coupled to an input of XOR gate 1283 via node 1279. An output of flip-flop 1263 is coupled to an input of XOR gate 1283 via node

1281. An output of XOR gate 1283 is coupled to an input of multiplexer 1243 via node

1285. A PRBS test signal is applied to a selection input 1241 of multiplexer 1243.

Odd-numbered bits from MSB receiver 1205 are passed to an input of multiplexer  
5 1243 and to an input of XOR gate 1247 via node 1207. The output of multiplexer 1243 is  
coupled to an input of XOR gate 1247 and to the serial data input of a shift register  
comprising flip-flops 1213, 1215, 1217, and 1219 via node 1245. An output of XOR gate  
1247 is provided at node 1249. A receive clock signal is provided to a clock input of the  
shift register via node 1209. An unload signal for providing parallel data outputs from  
10 the shift register is applied to the shift register via node 1211. Parallel data are provided  
at parallel data outputs 1221, 1223, 1225, and 1227 of flip-flops 1213, 1215, 1217, and  
1219, respectively.

An output of flip-flop 1219 is coupled to an input of XOR gate 1233 via node  
15 1229. An output of flip-flop 1213 is coupled to an input of XOR gate 1233 via node  
1231. An output of XOR gate 1233 is coupled to an input of multiplexer 1294 via node  
1235. A PRBS test signal is applied to a selection input 1292 of multiplexer 1294.

Even-numbered bits from LSB receiver 1206 are passed to an input of multiplexer  
20 1294 and to an input of XOR gate 1298 via node 1258. The output of multiplexer 1294 is  
coupled to an input of XOR gate 1298 and to the serial data input of a shift register  
comprising flip-flops 1264, 1266, 1268, and 1270 via node 1296. An output of XOR gate  
1298 is provided at node 1200. A receive clock signal is provided to a clock input of the  
shift register via node 1260. An unload signal for providing parallel data outputs from  
25 the shift register is applied to the shift register via node 1262. Parallel data are provided  
at parallel data outputs 1272, 1274, 1276, and 1278 of flip-flops 1264, 1266, 1268, and  
1270, respectively.

An output of flip-flop 1270 is coupled to an input of XOR gate 1284 via node  
30 1280. An output of flip-flop 1264 is coupled to an input of XOR gate 1284 via node

1282. An output of XOR gate 1284 is coupled to an input of multiplexer 1244 via node 1286. A PRBS test signal is applied to a selection input 1242 of multiplexer 1244.

Odd-numbered bits from LSB receiver 1206 are passed to an input of multiplexer 1244 and to an input of XOR gate 1248 via node 1208. The output of multiplexer 1244 is coupled to an input of XOR gate 1248 and to the serial data input of a shift register comprising flip-flops 1214, 1216, 1218, and 1220 via node 1246. An output of XOR gate 1248 is provided at node 1250. A receive clock signal is provided to a clock input of the shift register via node 1210. An unload signal for providing parallel data outputs from the shift register is applied to the shift register via node 1212. Parallel data are provided at parallel data outputs 1222, 1224, 1226, and 1228 of flip-flops 1214, 1216, 1218, and 1220, respectively.

An output of flip-flop 1220 is coupled to an input of XOR gate 1234 via node 1230. An output of flip-flop 1214 is coupled to an input of XOR gate 1234 via node 1232. An output of XOR gate 1234 is coupled to an input of flip-flop 1238 via node 1236. A receive clock signal is applied to a clock input 1237 of flip-flop 1238. An output of flip-flop 1238 is coupled to an input of multiplexer 1293 via node 1239. A PRBS test signal is applied to a selection input 1291 of multiplexer 1293.

Figure 13 is a logic diagram illustrating a quad Rambus signaling level (QRSL) receive circuit capable of operating in a PRBS test mode and a roll test mode in accordance with an embodiment of the invention. Pad 1301 is coupled to node 1302, which is coupled to most significant bits (MSB) receiver 1305 and least significant bits (LSB) receiver 1306. A receive clock signal is provided to MSB receiver 1305 at node 1303 and to LSB receiver 1306 at node 1304.

Even-numbered bits from MSB receiver 1305 are passed to an input of multiplexer 1393 and to an input of XOR gate 1397 via node 1357. The output of multiplexer 1393 is coupled to an input of XOR gate 1397 and to a serial data input of a shift register comprising flip-flops 1363, 1365, 1367, and 1369 via node 1395. An output

of XOR gate 1397 is provided at node 1399. A receive clock signal is provided to a clock input of the shift register via node 1359. An unload signal for providing parallel data outputs from the shift register is applied to the shift register via node 1361. Parallel data are provided at parallel data outputs 1371, 1373, 1375, and 1377 of flip-flops 1363, 1365, 1367, and 1369, respectively.

An output of flip-flop 1369 is coupled to an input of XOR gate 1383 and to an input of multiplexer 1393 via node 1379. An output of flip-flop 1363 is coupled to an input of XOR gate 1383 via node 1381. An output of XOR gate 1383 is coupled to an input of multiplexer 1343 via node 1385. A PRBS test signal is applied to a selection input 1341 of multiplexer 1343. A roll test signal is applied to a selection input 1387 of multiplexer 1343.

Odd-numbered bits from MSB receiver 1305 are passed to an input of multiplexer 1343 and to an input of XOR gate 1347 via node 1307. The output of multiplexer 1343 is coupled to an input of XOR gate 1347 and to the serial data input of a shift register comprising flip-flops 1313, 1315, 1317, and 1319 via node 1345. An output of XOR gate 1347 is provided at node 1349. A receive clock signal is provided to a clock input of the shift register via node 1309. An unload signal for providing parallel data outputs from the shift register is applied to the shift register via node 1311. Parallel data are provided at parallel data outputs 1321, 1323, 1325, and 1327 of flip-flops 1313, 1315, 1317, and 1319, respectively.

An output of flip-flop 1319 is coupled to an input of XOR gate 1333 and to an input of multiplexer 1343 via node 1329. An output of flip-flop 1313 is coupled to an input of XOR gate 1333 via node 1331. An output of XOR gate 1333 is coupled to an input of multiplexer 1394 via node 1335. A PRBS test signal is applied to a selection input 1392 of multiplexer 1394. A roll test signal is applied to a selection input 1390 of multiplexer 1394.

Even-numbered bits from LSB receiver 1306 are passed to an input of multiplexer 1394 and to an input of XOR gate 1398 via node 1358. The output of multiplexer 1394 is coupled to an input of XOR gate 1398 and to the serial data input of a shift register comprising flip-flops 1364, 1366, 1368, and 1370 via node 1396. An output of XOR gate 1398 is provided at node 1300. A receive clock signal is provided to a clock input of the shift register via node 1360. An unload signal for providing parallel data outputs from the shift register is applied to the shift register via node 1362. Parallel data are provided at parallel data outputs 1372, 1374, 1376, and 1378 of flip-flops 1364, 1366, 1368, and 1370, respectively.

An output of flip-flop 1370 is coupled to an input of XOR gate 1384 and to an input of multiplexer 1394 via node 1380. An output of flip-flop 1364 is coupled to an input of XOR gate 1384 via node 1382. An output of XOR gate 1384 is coupled to an input of multiplexer 1344 via node 1386. A PRBS test signal is applied to a selection input 1342 of multiplexer 1344. A roll test signal is applied to a selection input 1388 of multiplexer 1344.

Odd-numbered bits from LSB receiver 1306 are passed to an input of multiplexer 1344 and to an input of XOR gate 1348 via node 1308. The output of multiplexer 1344 is coupled to an input of XOR gate 1348 and to the serial data input of a shift register comprising flip-flops 1314, 1316, 1318, and 1320 via node 1346. An output of XOR gate 1348 is provided at node 1350. A receive clock signal is provided to a clock input of the shift register via node 1310. An unload signal for providing parallel data outputs from the shift register is applied to the shift register via node 1312. Parallel data are provided at parallel data outputs 1322, 1324, 1326, and 1328 of flip-flops 1314, 1316, 1318, and 1320, respectively.

An output of flip-flop 1320 is coupled to an input of XOR gate 1334 and to an input of multiplexer 1344 via node 1330. An output of flip-flop 1314 is coupled to an input of XOR gate 1334 via node 1332. An output of XOR gate 1334 is coupled to an input of flip-flop 1338 via node 1336. A receive clock signal is applied to a clock input

1337 of flip-flop 1338. An output of flip-flop 1338 is coupled to an input of multiplexer 1393 via node 1339. A PRBS test signal is applied to a selection input 1391 of multiplexer 1393. A roll test signal is applied to a selection input 1389 of multiplexer 1393.

5

Figure 14 is a timing diagram illustrating signals in accordance with an embodiment of the invention. A transmit circuit load signal 1401, a transmit circuit PRBS test signal 1402, a receive circuit PRBS test signal 1405, and an error signal 1406 are illustrated. A plurality of transmit circuit data 1403 and a plurality of receive circuit data 1404 are also illustrated.

10

Data are loaded into a shift register in the transmit circuit on the rising edge 1407 of pulse 1408 of the transmit circuit load signal 1401. A PRBS test mode is entered upon the assertion 1409 of the transmit circuit PRBS test signal 1402. Sufficient transmit circuit data 1403 to initialize the transmit circuit and the receive circuit to like states is communicated from the transmit circuit to the receive circuit, where it appears as receive circuit data 1404. Bits 1413, 1414, 1415, 1416, 1417, 1418, and 1419 of transmit circuit data 1403 are communicated to provide bits 1420, 1421, 1422, 1423, 1424, 1425, and 1426 of receive circuit data 1404 respectively. This data are communicated between time 1411 and time 1412, during period 1410, and serves to seed the receive circuit with appropriate data.

15

20

Once sufficient data has been communicated between the transmit circuit and the receive circuit, receive circuit PRBS test signal 1405 is asserted at assertion 1427. Then, between time 1429 and time 1430, during period 1428, testing may be performed using the seeded receive circuit data. If, during the testing, an element of transmit circuit data being transmitted to the receive circuit does not match a corresponding element of receive circuit data, error signal 1406 is asserted, such as occurs at assertions 1433 and 1434, which occur during period 1432 after time 1431. When testing is completed, the system may be returned to its normal mode by deasserting the transmit circuit PRBS test signal 1402 and the receive circuit PRBS test signal 1405.

25

30

In a manner similar to the PRBS test mode, a roll test mode may be entered by asserting a transmit circuit roll test signal (TX ROLL TEST) and a receive circuit roll test signal (RX ROLL TEST) in place of the transmit circuit PRBS test (TX PRBS TEST) and receive circuit PRBS test (RX PRBS TEST) signals illustrated in Figure 14.

Figure 15 is a block diagram illustrating a differential receiver that may be used in conjunction with an embodiment of the invention. Differential receiver 1501 comprises a non-inverting input 1502, an inverting input 1503, an offset input 1504, and an output 1505. Offset input 1504 may be implemented in various ways, for example, as a single-ended input or a differential input.

Figure 16 is a waveform diagram illustrating a differential signal that may be used in conjunction with an embodiment of the invention. The differential signal comprises a signal 1601 and its complementary signal 1602.

Figure 17 is a waveform diagram illustrating a differential signal that may be used in conjunction with an embodiment of the invention. The differential signal comprises a signal 1701 and its complementary signal 1702. The signal 1701 and its complementary signal 1702 have been shifted slightly relative to each other, for example through the use of offset input 1504 of Figure 15.

Figure 18 is a waveform diagram illustrating a differential signal that may be used in conjunction with an embodiment of the invention. The differential signal comprises a signal 1801 and its complementary signal 1802. The signal 1801 and its complementary signal 1802 have been shifted substantially relative to each other, for example through the use of offset input 1504 of Figure 15.

Figure 19 is a schematic diagram illustrating an example of an input stage of an offsetable differential receiver in accordance with an embodiment of the invention. A differential input signal is coupled to an input 1901 at a gate of a first input transistor



1903 and to an input 1902 at a gate of a second input transistor 1904. A source of the first input transistor and a source of the second input transistor are coupled to a first terminal 1919 of current source 1920. A second terminal 1921 of current source 1920 is coupled to ground.

5

A drain of the first input transistor 1903 is coupled to the drain of transistor 1917, to a first terminal of resistor 1907, and to a first output. A drain of the second input transistor 1904 is coupled to the drain of transistor 1918, to a first terminal of resistor 1908, and to a second output. The second end of the first resistor is coupled to a voltage reference 1905. The second end of the second resistor is coupled to a voltage reference 1906. The sources of transistors 1917 and 1918 are coupled to a first terminal 1919 of a variable current source 1920. The second terminal 1921 of variable current source 1920 is coupled to ground.

15 A shifting input signal 1914 is applied to the gate of transistor 1917. The shifting input signal 1914 is inverted by inverter 1915 and applied to the gate terminal 1916 of transistor 1918.

Figure 20 is a schematic diagram illustrating an example of an input stage of an offsetable differential receiver in accordance with an embodiment of the invention. A differential input signal is coupled to an input 2001 at a gate of a first input transistor 2003 and to an input 2002 at a gate of a second input transistor 2004. A source of the first input transistor and a source of the second input transistor are coupled to a first terminal 2019 of current source 2020. A second terminal 2021 of current source 2020 is coupled to ground.

A drain of the first input transistor 2003 is coupled to the drain of transistor 2017, to a first terminal of resistor 2007, and to a first output. A drain of the second input transistor 2004 is coupled to the drain of transistor 2018, to a first terminal of resistor 2008, and to a second output. The second end of the first resistor is coupled to a voltage reference 2005. The second end of the second resistor is coupled to a voltage reference

2006. The sources of transistors 2017 and 2018 are coupled to a first terminal 2019 of a current source 2020. The second terminal 2021 of current source 2020 is coupled to ground. A shifting input signal 2014 is applied to the gate of transistor 2017. A fixed DC voltage 2016 is applied to the gate terminal of transistor 2018. Alternatively, a variable signal, such as a variable voltage, may be applied to the gate terminal of transistor 2018. As one example, the variable signal at the gate terminal of transistor 2018 may vary complementary to the shifting input signal 2014. This would allow, for example, a differential signal to be used to control the offset. Alternatively, the signal at the gate terminal of transistor 2018 may vary independent of the shifting input signal 2014.

Figure 21 is a waveform diagram illustrating the shifting of an offset for a differential signal in accordance with an embodiment of the invention. Waveform 2101 may be shifted to yield waveforms 2102, 2103, 2104, and 2105. Waveform 2106 may be shifted to yield waveforms 2107, 2108, 2109, and 2110. Intersections between the waveform, such as intersections 2111, 2112, 2113, 2114, 2115, 2116, 2117, 2118, 2119, 2120, 2121, 2122, 2123, 2124, 2125, 2126, 2127, 2128, and 2129 can be evaluated to determine a difference between the waveforms.

Figure 22 is a waveform diagram illustrating a waveform obtained by determining a difference between waveforms. The waveform may be obtained based in the intersections depicted in Figure 21 based on the equation  $A - B + \text{offset}$ .

Figure 23 is a flow diagram illustrating a method in accordance with an embodiment of the invention. The method begins in step 2301. In step 2302, a transmit repeating pattern is generated in a transmit circuit. Step 2302 may include step 2303. In step 2303, a shift register may be utilized to generate the transmit repeating pattern. Step 2303 may include step 2304. In step 2304, a linear feedback shift register (LFSR) may be utilized to generate the transmit repeating pattern.

From step 2302, the method continues to step 2305. In step 2305, a transmit repeating pattern is transmitted to a receive circuit. Step 2305 may include steps 2306, 2307, and/or 2308. In step 2306, the transmit repeating pattern is transmitted as a signal referenced to a ground. In step 2307, the transmit repeating pattern is transmitted as a differential signal over a pair of conductors. In step 2308, the transmit repeating pattern is transmitted by encoding two bits of information on a single conductor simultaneously. From step 2305, the method continues to step 2309. In step 2309, a receive repeating pattern is generated in the receive circuit. From step 2309, the method continues to step 2310. In step 2310, the transmit repeating pattern is compared to the receive repeating pattern to obtain a comparison. From step 2310, the method continues to step 2311. In step 2311, a parameter affecting operation of the transmit circuit based on the comparison is adjusted. From step 2311, the method either continues to step 2312, where it ends, or it returns to step 2302 and performs one or more additional iterations, allowing the effects of adjustments performed in step 2311 to be assessed and further optimization to occur. Such iterations may continue to occur without limit.

Figure 24 is a waveform diagram illustrating an example of a persistent display of overlapping samples of a waveform in accordance with an embodiment of the invention. One embodiment of the invention may be used to provide information similar to that which is traditionally obtainable through the use of an oscilloscope. In the test mode, comparison can be made between a pattern generated in the transmit circuit and a pattern generated in the receive circuit. This testing can be reiterated for different receiver timing and overdrive conditions while the signal representing the pattern is being compared. When the time and overdrive condition of the receiver is varied to the region where the pattern comparisons yield inconsistent results, the failing region corresponds to a metastable region of the receiver. When these metastable regions are plotted, they outline the signal waveform that is being received at the receiver, including the signal uncertainty (jitter) and the receiver timing and overdrive deadband requirement.

Hence, the outline of these metastable regions represent the signal as seen by the receiver with its own receiving characteristics. With this capability of visualizing the

signal, various effects on the signal can be checked out. For example, an output current level, crosstalk, attenuation, etc. In case of unwanted signal integrity behaviors, different compensation techniques can be used to reduce or eliminate those behaviors.

5           The example of Figure 24 illustrates samples of waveforms exhibiting the effects of crosstalk induced by other nearby conductors, as can be seen, for example at locations 2401, 2402, 2403, and 2404.

10           Figure 25 is a waveform diagram illustrating an example of a persistent display of overlapping samples of a waveform in accordance with an embodiment of the invention. The example of Figure 25 illustrates results obtained using integrating receivers in the receive circuit. The effects of crosstalk seen at locations 2501, 2502, 2503, and 2504 can be seen to be reduced relative to Figure 24.

15           Figure 26 is a waveform diagram illustrating an example of a persistent display of overlapping samples of a waveform in accordance with an embodiment of the invention. The example of Figure 26 shows results obtained using "step response" types of waveforms. Locations 2601 and 2602 illustrate effects of an impedance discontinuity in the medium between the transmit circuit and the receive circuit.

20           Figure 27 is a waveform diagram illustrating an example of a persistent display of overlapping samples of a waveform in accordance with an embodiment of the invention. The example of Figure 27 illustrated a 4-level pulse amplitude modulation (4-PAM) generated using patterns representing a stair-step-type signal. Differences between the  
25           rising edges 2701, 2702, 2703, 2704, 2705, and 2706 and their respective falling edges 2707, 2708, 2709, 2710, 2711, and 2712 are observable.

30           Figure 28 is a waveform diagram illustrating an example of a persistent display of overlapping samples of a waveform in accordance with an embodiment of the invention. The example of Figure 28 illustrates samples of waveforms showing effects of crosstalk on a conductor that is held at an otherwise constant level. While ideally the display

would be merely a flat line 2810, the effects of crosstalk induced on the conductor are observable at locations 2801, 2802, 2803, 2804, 2805, 2806, 2807, 2808, and 2809.

Figure 29 is a waveform diagram illustrating an example of a persistent display of overlapping samples of a waveform in accordance with an embodiment of the invention. The example of Figure 29 illustrates an effect observable at location 2901 cause by other conductors in close proximity switching at the same frequency as the signal representing the pattern generated in the transmit circuit.

Thus, in view of Figures 24-29, it can be seen that an embodiment of the invention provides a powerful tool for *in-situ* characterization and optimization of signaling systems. Characteristics that could not be determined using traditional test equipment are readily ascertainable in accordance with an embodiment of the invention.

Figure 30 is a block diagram illustrating a system in accordance with an embodiment of the invention. The system comprises transmit circuit 3001, medium 3002, and receive circuit 3003. Transmit circuit 3001 comprises a shift register 3005 having a parallel load input 3004. A feedback loop 3006 couples a serial data output of shift register 3005 to a serial data input of shift register 3005. The serial data output of shift register 3005 is also coupled to an input of transmitter 3015. An output of transmitter 3015 is coupled to medium 3002.

Receiver circuit 3003 comprises receiver 3016, multiplexer 3019, shift register 3008, and XOR gate 3013. Medium 3002 is coupled to an input of receiver 3016. A receive circuit timing signal is coupled to an input of receiver 3016 at node 3017. A voltage reference signal is coupled to an input of receiver 3016 at node 3018. An output of receiver 3016 is coupled to an input of multiplexer 3019 and to an input of XOR gate 3013. A fill pipe signal is coupled to a selection input of multiplexer 3019 at node 3020. An output of multiplexer 3019 is coupled to a serial data input of shift register 3008. A serial data output of shift register 3008 is coupled to an input of multiplexer 3019 and to

an input of XOR gate 3013. An output of XOR gate 3013 provides an error output at node 3014.

Figure 31 is a flow diagram illustrating a method in accordance with an embodiment of the invention. The method begins in step 3101 and continues to step 3102. In step 3102, some or all of steps 2302 through 2310 of Figure 23 are performed. From step 3102, the method proceeds to step 3103. In step 3103, a determination is made as to whether or not receiver characteristics should be changed. If so, the method proceeds to step 3104. If not, the method returns to step 3102. In step 3104, one or more receiver characteristics are changed. These receiver characteristics may include a receive circuit timing signal and a voltage reference.

From step 3104, the method continues to step 3105. In step 3105, boundary values of the receiver characteristic are determined within which reliable operation of the system is provided. From step 3105, the method continues to step 3106. In step 3106, a determination is made as to whether or not system parameters are to be adjusted. If so, the method continues to step 3107. If not, the method returns to step 3102. In step 3107, system parameters are adjusted. Such system characteristics may include an output current, a crosstalk cancellation coefficient, and a self-equalization coefficient. From step 3107, the method returns to step 3102 and is repeated.

While embodiments of the invention have been described in reference to signaling systems generally, it should be understood that the invention may be applied to various types of signaling systems in various contexts. As an example, the invention may be implemented in a signaling system existing within a memory system. For example, an embodiment of the invention may be provided where either or both of the transmit circuit and the receive circuit are incorporated in either or both of a memory controller and a memory device. Thus, signaling relating to memory operations within the memory system may be evaluated and optimized. The term signaling is understood to be broadly applicable. Even within the specific context of a memory system, signaling is understood to refer to any type of signals that may exist, for example, address signals, control

